

# Transparent indium gallium zinc oxide transistor based floating gate memory with platinum nanoparticles in the gate dielectric

Arun Suresh, Steven Novak, Patrick Wellenius, Veena Misra, and John F. Muth<sup>a)</sup>  
 Department of ECE, North Carolina State University, Raleigh, North Carolina 27695, USA

(Received 10 November 2008; accepted 5 March 2009; published online 23 March 2009)

A transparent memory device has been developed based on an indium gallium zinc oxide thin film transistor by incorporating platinum nanoparticles in the gate dielectric stack as the charge storage medium. The transfer characteristics of the device show a large clockwise hysteresis due to electron trapping and are attributed to the platinum nanoparticles. Effect of the gate bias stress (program voltage) magnitude, duration, and polarity on the memory window characteristics has been studied. Charge retention measurements were carried out and a loss of less than 25% of the trapped electrons was observed over  $10^4$  s indicating promising application as nonvolatile memory. © 2009 American Institute of Physics. [DOI: 10.1063/1.3106629]

The field of transparent electronics offers the opportunity to develop optoelectronic devices for “see-through” display technologies and other applications.<sup>1</sup> A key element to realize transparent circuits is a transparent thin film transistor (TTFT).<sup>2</sup> Recently, amorphous oxide semiconductors (AOSs), using wide band-gap oxides have been developed for TTFT channel application. These oxides are transparent to visible light and have higher mobilities ( $\sim 10\text{--}30\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ ) compared to conventional *a*-Si:H and organic materials ( $\sim 0.1\text{--}1\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ ).<sup>3</sup> AOSs can also be deposited at room temperature allowing them to be deposited on flexible plastic substrates. There have been several reports of transparent transistors based on zinc oxide,<sup>4</sup> zinc tin oxide,<sup>5</sup> indium gallium zinc oxide (IGZO),<sup>6</sup> and other semiconducting oxide thin films. The bulk of the research focus has been on enhancing key TFT performance metrics, however, to extend the concept of transparent transistors to transparent circuits and electronics, it is useful to investigate other circuit components such as transparent diodes<sup>7</sup> and memory elements.<sup>8</sup> In this paper we report the development and demonstration of a transparent nonvolatile memory device consisting of a transparent floating gate transistor that incorporates platinum nanoparticles (Pt-NPs) which act as the charge-trapping medium in the gate dielectric. This integration of a TTFT with memory functionality can open up different pixel circuit or memory cell designs.<sup>9</sup>

Nonvolatile memory based on a floating gate device structure has been widely utilized in silicon-based electronics.<sup>10</sup> In these structures the floating gate is used to store and release charge with the memory state represented by a shift in the threshold voltage. A large research effort has been ongoing to replace the current poly-Si floating gate with a memory-cell structure using discrete traps or nanoparticles as the charge storage media.<sup>11</sup> Numerous material approaches have been proposed, i.e., semiconductor (Si, Ge, etc.), redox active molecule,<sup>12</sup> metal (Au, Pt, etc.), and dielectric ( $\text{Al}_2\text{O}_3$ ,  $\text{Si}_3\text{N}_4$ , etc.) nanoparticles.<sup>13</sup> The memory structure based on metal nanoparticles possesses several advantages over conventional floating gate memories, such as a larger trapping probability, a stronger coupling with the con-

duction channel, and a wide range of available work functions, and in case of defects in the control/tunnel oxide the discrete traps ensure a larger probability of charge retention.<sup>14</sup> These memory device approaches are typically on rigid silicon substrates and are not compatible with flexible substrates and transparent electronic schemes.

The schematic cross-section of the IGZO memory device is shown in Fig. 1(a). Commercial glass substrates coated with 250 nm sputtered indium tin oxide (ITO) and 220 nm atomic layer deposition (ALD)  $\text{AlO}_x\text{--TiO}_x$  superlattice (ATO) were used.<sup>15</sup> ITO acts as the gate electrode and the ATO as the dielectric (blocking oxide) of the device. Pt-NPs were formed on the ATO dielectric at 270 °C by ALD.<sup>16</sup> The number of cycles was optimized for the  $\text{AlO}_x$  interface (the ATO dielectric is capped on both ends by  $\text{AlO}_x$ ) to get the desired size and distribution.<sup>16</sup> A thin layer  $\sim 5$  nm of  $\text{AlO}_x$ , which acts as the tunneling oxide, was deposited at 200 °C by ALD. This was followed by the deposition and patterning of IGZO (channel) and ITO (source/drain) by pulsed laser deposition (PLD) at room temperature.<sup>6</sup> Control samples without the Pt-NPs (ITO/ATO/ $\text{AlO}_x$ /IGZO/ITO) were also fabricated for comparison purposes. The fabricated devices were post-annealed at 250 °C in atmosphere for 1 h. The TTFT memory device characteristics were measured in the dark with an HP 4155B semiconductor parameter analyzer.

The raw optical transmission versus the wavelength of the substrate and the entire IGZO memory device stack is shown in Fig. 1(a). At visible wavelengths the entire stack was still highly transparent throughout the visible spectrum. The addition of the Pt-NPs,  $\text{AlO}_x$ , IGZO, and ITO layers did not cause an appreciable reduction in the transparency of the device. A cross-sectional transmission electron micrograph (TEM) of the IGZO memory device is shown in Fig. 1(b). The inset clearly shows the presence of Pt-NPs about 3 nm in size. Under similar deposition conditions on smooth  $\text{AlO}_x$  coated silicon substrates, AFM images show a Pt-NP size of 3–4 nm.

The transfer characteristics [ $\log(I_{\text{DS}})\text{--}V_{\text{GS}}$ ] of the IGZO TTFTs both with and without Pt-NPs are shown in Figs. 2(a) and 2(b). The gate voltage  $V_{\text{G}}$  was swept in 0.2 V increments from a negative value to a positive value and back to the starting negative value (e.g.,  $-10$  to  $10$  to  $-10$  V), while the

<sup>a)</sup>Electronic mail: muth@unity.ncsu.edu.

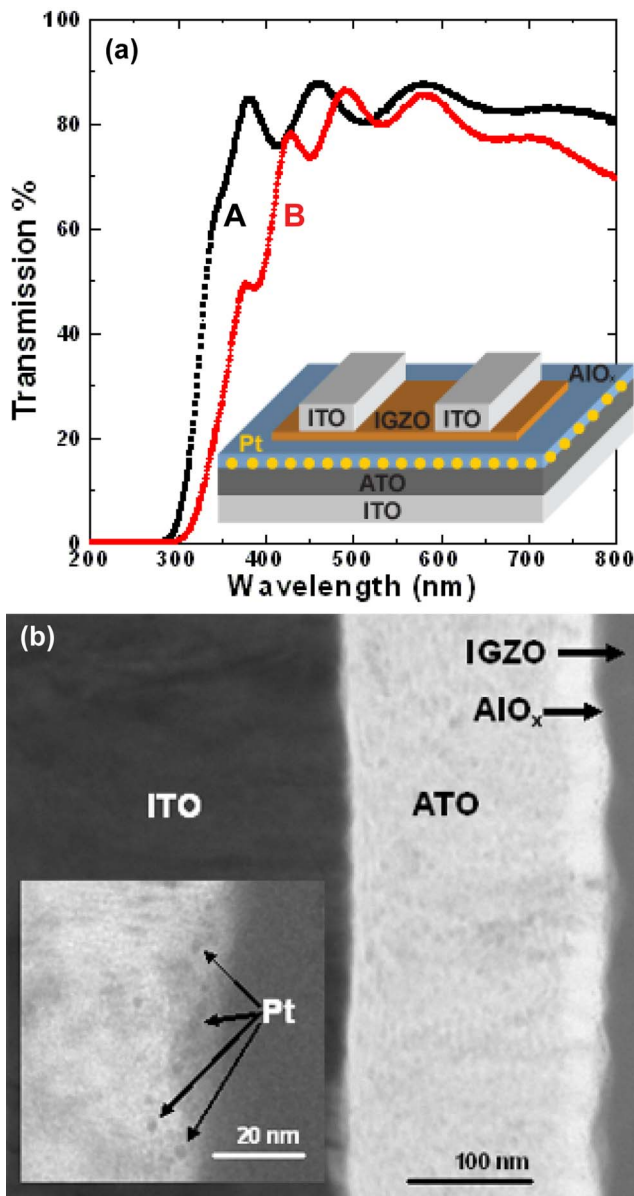


FIG. 1. (Color online) (a) Comparison of the optical transmission spectrum of (A) the substrate (glass/ITO/ATO) and (B) the entire stack of the memory device (glass/ITO/ATO/Pt-NCs/AIO<sub>x</sub>/IGZO/ITO). The inset is the schematic cross-section of the IGZO memory TTFT. (b) Cross-section TEM micrograph of a TTFT memory stack and the inset shows the presence of embedded Pt-NPs.

source/drain voltage  $V_{DS}$  was fixed at 10 V. We define the TTFT turn-on voltage,  $V_{on}$ , as the gate voltage where the drain current reaches 100 pA. We can see in Fig. 2(a) that the control transistors (without the Pt-NPs) show negligible hysteresis with the  $\Delta V_{on}[V_{on}(\text{reverse sweep}) - V_{on}(\text{forward sweep})] \sim 0.35$  V when the device was swept from  $-30$  to  $30$  V and back. The following TFT characteristics were extracted for the control devices,  $V_i = -0.25$  V,  $\mu_{eff} = 14$  cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>,  $I_{on}/I_{off} > 10^7$ , and  $S = 0.2$  V decade<sup>-1</sup>.

In contrast, a significant hysteresis phenomenon can be seen in the devices with embedded Pt-NPs, as shown in Fig. 2(b). We see a clockwise hysteresis of the transfer curves. IGZO TTFTs are basically *n*-type devices and a positive bias generates an accumulation layer of electrons in the channel close to the channel/dielectric interface. These electrons tunnel through the AIO<sub>x</sub> (tunneling oxide) and get trapped in the

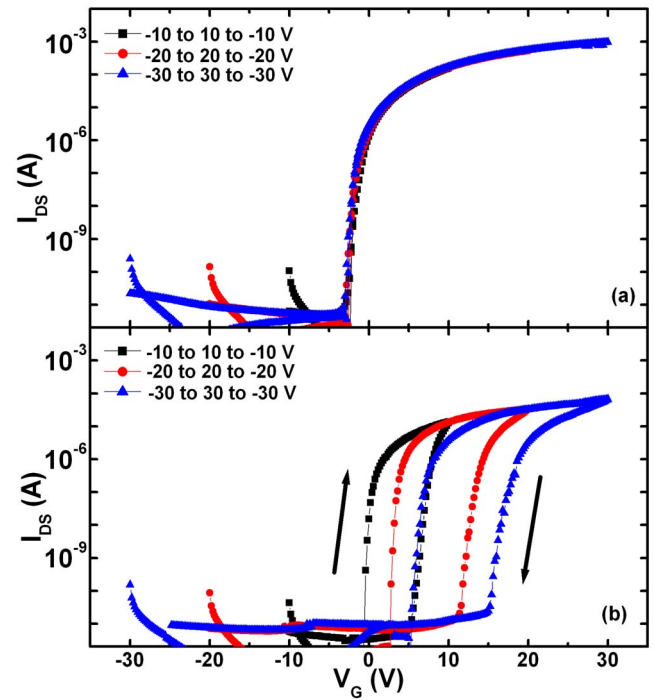


FIG. 2. (Color online) (a)  $\log(I_{DS})$ - $V_{GS}$  sweeps of (a) control TFT (no Pt-NPs) and (b) memory TFT (with Pt-NPs). Hysteresis sweeps (■)  $-10$  to  $-10$  V, (●)  $-20$  to  $20$  to  $-20$  V, and (▲)  $-30$  to  $30$  to  $-30$  V were made consecutively. The directions of the forward and reverse sweeps are indicated.  $V_{DS} = 10$  V and TFT dimensions:  $L = 100$   $\mu\text{m}$  and  $W = 400$   $\mu\text{m}$ .

Pt-NPs when  $V_G > 0$  during the forward sweep. During the reverse sweep the trapped electrons screen the applied gate voltage leading to a lower current and the observed clockwise hysteresis in the transfer characteristics. For the same reason the maximum current seen in the devices with Pt-NPs is about an order of magnitude lower than the control devices due to the electrons trapped in the Pt-NPs. We can also notice that the subthreshold slopes of both the forward and the reverse sweeps are similar indicating no defect creation at the semiconductor/dielectric interface due to the charging process. We also observed that the slope of the  $\sqrt{I_{DS}}$  versus  $V_G$  characteristics does not change appreciably when the device was charged showing that the charging process has a minimal influence on the carrier mobility.

From Fig. 2(b) we can see that  $\Delta V_{on}$  increases by 5.1, 8.9, and 9.8 V as the  $V_G$  sweep range increases from  $(-10$  to  $10$  to  $-10$  V),  $(-20$  to  $20$  to  $-20$  V), and  $(-30$  to  $30$  to  $-30$  V), respectively, showing that the trapping sites are not completely saturated. The  $I_{off}$  of the reversely swept curves are higher than that of the forward swept curves indicating that the trapped electrons are not released in the reverse sweep.<sup>17</sup> We observe that the  $V_{on}$  of the forward sweep for the three consecutive sweeps,  $(-10$  to  $10$  to  $-10$  V),  $(-20$  to  $20$  to  $-20$  V), and  $(-30$  to  $30$  to  $-30$  V), increases, also indicating the trapped electrons are not completely released during the reverse sweep. This is the result of the device being in a depletion mode when a negative gate bias is applied ( $V_G < 0$ ), hence the device would require a much larger time and/or negative potential to completely remove the trapped electrons.<sup>18</sup>

The charging efficiency of the Pt-NPs was verified by stressing the memory devices with a gate bias. Both positive and negative bias (program voltage) for a predetermined

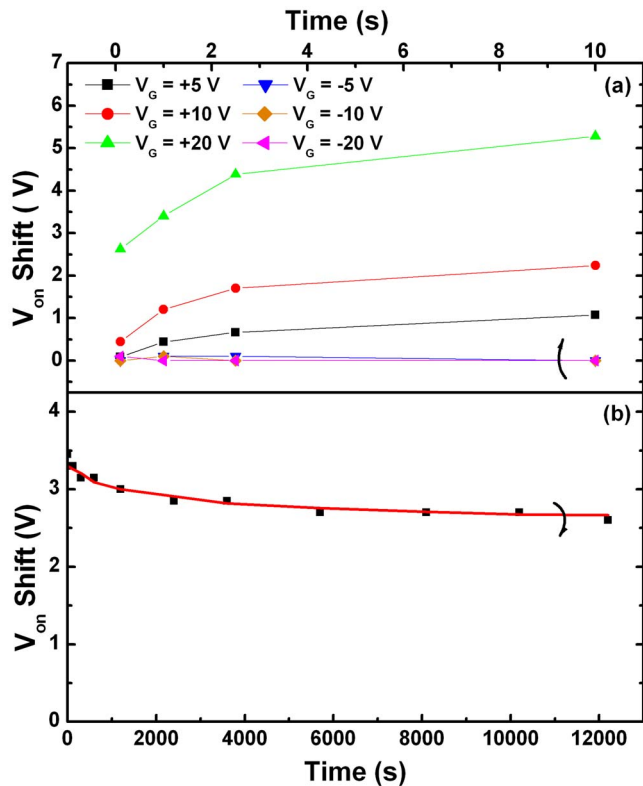


FIG. 3. (Color online) (a) Shift in  $V_{on}$  as a function of gate bias and the stress duration (top abscissa) for positive and negative gate bias. Source and drain electrodes were grounded, while stressing the gate.  $V_{DS}=10$  V, while reading the device. (b) Charge retention characteristics (bottom abscissa) of the IGZO memory TFT after stressing at  $V_G=20$  V for 2 s. The curves are for visual aid.

time (0.1, 1, 2.5, and 10 s) was applied to the gate electrode, while grounding the source and drain electrodes. The  $V_{on}$  was measured before and after the application of the stress and the shift in  $V_{on}$  is plotted in Fig. 3(a). A positive gate bias induces a positive  $V_{on}$  shift as expected due to the electron injection into the charge-trapping layer. The hysteresis memory window [ $\Delta V_{on}=V_{on}(\text{post})-V_{on}(\text{pre})$ ] increases with an increase in the applied gate bias and the stress duration. The shift in  $V_{on}$  tends to saturate for stress times above 3 s indicating that the number of electrons the nanoparticle can store is saturating.<sup>19</sup> On the other hand a negative gate bias does not introduce a shift in  $V_{on}$ . The invariability of  $V_{on}$  with a negative bias on the gate can be explained by the lack of electrons in the channel due to the creation of the depletion layer and lack of holes, which are not generated in the semiconductor. This shows that in this device programming is done by electron trapping, while programming with holes is not possible.<sup>20</sup> The control TFTs (without the Pt-NPs) showed minimal ( $\sim 0.2$  V for +20 V bias for 10 s) variation in  $V_{on}$  with a positive gate bias and no shift in  $V_{on}$  for a negative gate bias confirming that the observed behaviors of the IGZO memory devices are due to trapping of electrons in the Pt-NPs.

The charge retention characteristics of the IGZO TTFT memory device were evaluated. The stored electron charge loss (measured as shift in  $V_{on}$ ) was assessed at room temperature after stressing the device at  $V_G=20$  V for 2 s, while the source and the drain electrodes were grounded. The  $V_{on}$  was measured periodically by sweeping  $V_G$  over 5 V around the

point when the TFT turns on to limit the charging effect during the read measurements.  $\Delta V_{on}$  as a function of time is shown in Fig. 3(b). Immediately after the stressing  $\Delta V_{on}$  is 3.45 V and within the first 500 s, it drops down to  $\sim 3$  V and then slowly reduces to 2.65 V after  $10^4$  s, which amounts to a 25% charge loss. The initial loss corresponds to electrons trapped in shallow interface states created during the Pt-NPs incorporation in the TFT dielectric, while the majority of the electrons are strongly trapped at the Pt-NP sites. Fitting the charge retention data to a logarithmic decay function, it was found that 50% charge retention was maintained for up to  $10^7$  s. Further improvements in the device behavior are expected if the blocking oxide ATO's thickness is reduced. This would lower the voltage requirements of the device leading to further optimization of the device structure.

In summary we have demonstrated a transparent memory device utilizing Pt-NPs in an AOS TTFT based on IGZO. The charge trapping is attributed to the presence of Pt-NPs and verified from the hysteresis of the TFT transfer characteristics. Electron injection was found under positive gate voltage stress, whereas holes cannot be injected due to the IGZO characteristics. The charge retention of the Pt-NPs was maintained with only a 25% loss after  $10^4$  s. The development of a memory device that can be integrated with other transparent circuit elements potentially offers additional functionality and design freedom for system-on-panel applications for transparent displays.

- <sup>1</sup>S. Ju, A. Facchetti, Y. Xuan, J. Liu, F. Ishikawa, P. Ye, C. Zhou, T. J. Marks, and D. B. Janes, *Nat. Nanotechnol.* **2**, 378 (2007).
- <sup>2</sup>J. F. Wager, *Science* **300**, 1245 (2003).
- <sup>3</sup>K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, *Nature (London)* **432**, 488 (2004).
- <sup>4</sup>P. Barquinha, E. Fortunato, A. Gonçalves, A. Pimentel, A. Marques, L. Pereira, and R. Martins, *Superlattices Microstruct.* **39**, 319 (2006).
- <sup>5</sup>H. Q. Chiang, J. F. Wager, R. L. Hoffman, J. Jeong, and D. A. Keszler, *Appl. Phys. Lett.* **86**, 013503 (2005).
- <sup>6</sup>A. Suresh, P. Wellenius, A. Dhawan, and J. F. Muth, *Appl. Phys. Lett.* **90**, 123512 (2007).
- <sup>7</sup>A. Kudo, H. Yanagi, K. Ueda, H. Hosono, H. Kawazoe, and Y. Yano, *Appl. Phys. Lett.* **75**, 2851 (1999).
- <sup>8</sup>H. Yin, S. Kim, C. J. Kim, I. Song, J. Park, S. Kim, and Y. Park, *Appl. Phys. Lett.* **93**, 172109 (2008).
- <sup>9</sup>H. Kimura, T. Maeda, T. Tsunashima, T. Morita, H. Murata, S. Hirota, and H. Sato, *SID Int. Symp. Digest Tech. Papers* **32**, 268 (2001).
- <sup>10</sup>F. M. Yang, T. C. Chang, P.-T. Liu, Y. H. Yeh, Y. C. Yu, J. Y. Lin, S. M. Sze, and J. C. Lou, *Thin Solid Films* **516**, 360 (2007).
- <sup>11</sup>C.-C. Wang, C.-S. Liang, J.-Y. Tseng, and T.-B. Wu, *Appl. Phys. Lett.* **90**, 182101 (2007).
- <sup>12</sup>S. Sarkar, A. Suresh, F. B. Myers, J. F. Muth, and V. Misra, *Appl. Phys. Lett.* **92**, 223304 (2008).
- <sup>13</sup>Y. Zhu, B. Li, J. Liu, G. F. Liu, and J. A. Yarmoff, *Appl. Phys. Lett.* **89**, 233113 (2006).
- <sup>14</sup>F. M. Yang, T. C. Chang, P. T. Liu, P. H. Yeh, Y. C. Yu, J. Y. Lin, S. M. Sze, and J. C. Luo, *Appl. Phys. Lett.* **90**, 132102 (2007).
- <sup>15</sup>ITO/ATO substrates supplied by Planar Systems Inc. Espoo, Finland, art\_pakkala@planar.com.
- <sup>16</sup>S. Novak, B. Lee, and V. Misra, "Platinum nano-particles grown by atomic layer deposition for non-volatile charge storage memory applications" (unpublished).
- <sup>17</sup>Y. Kuo and H. Nominanda, *Appl. Phys. Lett.* **89**, 173503 (2006).
- <sup>18</sup>C. Novembre, D. Guerin, K. Lmimouni, C. Gamrat, and D. Vuillaume, *Appl. Phys. Lett.* **92**, 103314 (2008).
- <sup>19</sup>J. H. Kim, K. H. Baek, C. K. Kim, Y. B. Kim, and C. S. Yoon, *Appl. Phys. Lett.* **90**, 123118 (2007).
- <sup>20</sup>W.-R. Chen, T.-C. Chang, P.-T. Liu, C.-H. Tu, J.-L. Yeh, Y.-T. Hsieh, R.-Y. Wang, and C.-Y. Chang, *Surf. Coat. Technol.* **202**, 1333 (2007).