

## Room temperature pulsed laser deposited indium gallium zinc oxide channel based transparent thin film transistors

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Indium gallium zinc oxide deposited by pulsed laser deposition at room temperature was used as a channel layer to fabricate transparent thin film transistors with good electrical characteristics: field effect mobility of  $11 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and subthreshold voltage swing of  $0.20 \text{ V/decade}$ . By varying the oxygen partial pressure during deposition the conductivity of the channel was controlled to give a low off-current of  $\sim 10 \text{ pA}$  and a drain current on/off ratio of  $\sim 5 \times 10^7$ . Changing the channel layer thickness was a viable way to vary the threshold voltage. The effect of the gate dielectric on the electrical behavior was also explored. © 2007 American Institute of Physics.

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There is substantial interest in the use of amorphous transparent conducting oxides for the channel of thin film transistors.<sup>1-3</sup> In addition to their transparency at visible wavelengths they have also been shown to have surprisingly high electron mobilities compared to more traditional amorphous semiconductors such as *a*-Si:H and organic semiconductors. In the amorphous phase, the mechanical properties are such that these materials have been demonstrated on flexible substrates.<sup>4</sup>

Transparent oxide semiconductors can be broadly divided into two categories, single component systems such as zinc oxide,<sup>5-7</sup> tin oxide,<sup>8</sup> and multicomponent systems including zinc indium oxide,<sup>9</sup> zinc tin oxide,<sup>10</sup> indium gallium oxide,<sup>11</sup> and indium gallium zinc oxide (IGZO).<sup>2,12</sup> Although stoichiometry control of the multicomponent oxides can be more difficult there are several advantages. The choice of alloys can be used to tailor the band gap. In the case of ZnO, which forms polycrystalline phases very easily even at room temperature, the addition of an element such as indium will inhibit the nucleation of polycrystalline grains. In terms of the long term stability of the materials, one can also expect that some alloy combinations will be more stable than other combinations. The remarkable feature of these materials is that while they do not have extremely high electron mobilities in crystalline form, the electron mobility remains nearly unchanged even as the atomic disorder is increased in polycrystalline and amorphous forms. Even when the material is truly amorphous the electron mobility can be more than an order of magnitude higher ( $10\text{--}50 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ) than conventional amorphous materials, which have electron mobilities  $< 1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ . The origin of the high mobility has been attributed to the high degree of overlap of the spherically symmetric cation orbitals that make up the conduction band.

Previous *a*-IGZO based thin film transistors (TFTs) fabricated on plastic substrates demonstrated the potential for IGZO TFTs but showed relatively low on/off current ratios and mobility.<sup>2</sup> More recently rf-magnetron sputtered *a*-IGZO TFTs have also been reported.<sup>12</sup> Our focus in this letter is examining the channel properties of IGZO based TFTs and

showing that they are controllable via deposition parameters, channel thickness, and choice of gate dielectric.

In this study, IGZO TTFTs were fabricated on glass substrates coated with a 200 nm sputtered ITO (sheet resistance of  $8 \Omega/\square$ ) and a 220 nm atomic layer deposited  $\text{AlO}_x$  and  $\text{TiO}_x$  (ATO) superlattice with  $\text{AlO}_x$  capped on both sides.<sup>13</sup> Indium tin oxide (ITO) acts as the gate electrode for our TFT structure and ATO as the dielectric layer. The TFTs fabricated for this study were a bottom-gated structure with the IGZO channel deposited at room temperature by pulsed laser deposition (PLD) using a homemade target. A commercial ITO target was ablated to deposit the source and the drain electrodes (typically of  $\sim 200 \text{ nm}$  thick) using room temperature PLD. The channel and the source/drain electrode layers were patterned using standard photolithography and lift-off techniques. The growth conditions for the channel layer (IGZO), especially the oxygen partial pressure during deposition and the number of pulses, were varied and optimized to give the required carrier concentration and thickness of the film. As a comparison we also evaluated silicon nitride

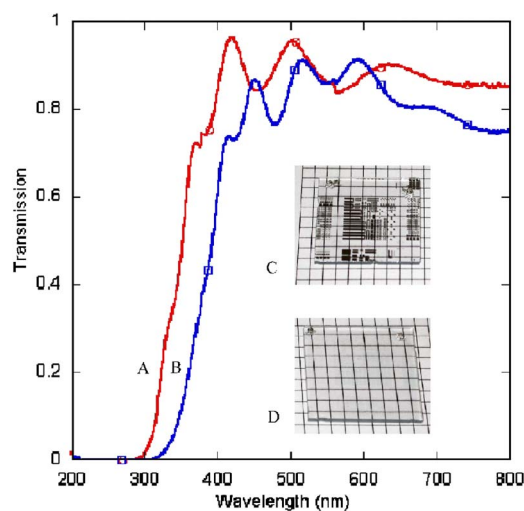


FIG. 1. (Color online) Optical transmission spectrum for the IGZO TFT stack. (A) without ITO source/drain layer and (B) with an ITO source/drain layer. The high transmission through out the visible spectrum can be seen in insets C and D, showing functioning transistors with C having opaque metal source/drain contacts and D having transparent contacts.

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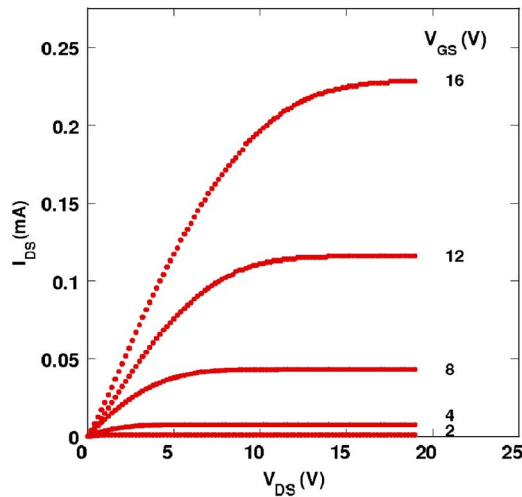


FIG. 2. (Color online) Drain current–drain voltage ( $I_{DS}$ - $V_{DS}$ ) characteristics for an IGZO TFT with ATO gate dielectric. IGZO channel deposited at oxygen partial pressure of 25 mTorr and thickness of 50 nm. TFT dimensions:  $L=100\ \mu\text{m}$  and  $W=400\ \mu\text{m}$ .

( $\text{SiN}_x$ ) as a gate dielectric, deposited using plasma enhanced chemical vapor deposition (PECVD) on commercial ITO substrates. The capacitance of the gate dielectric (ATO and  $\text{SiN}_x$ ) was measured using a standard  $C$ - $V$  meter, and an HP4145 parameter analyzer was used to measure the dc  $I$ - $V$  characteristics of the TFTs. All measurements were carried out in double-sweep mode; the gate voltage was swept up and then back down for each drain voltage.

Figure 1 shows the optical transmittance spectrum versus wavelength of the entire IGZO-TFT stack. The data represent raw transmission through the entire structure, i.e., the measured transmission is not corrected for either reflection or absorption. The entire stack was highly transparent at visible wavelengths and the majority of the absorption coming from the ITO contact layer which was deposited at room temperature. Depositing this layer at elevated temperatures would further improve the transparency, but was not done since the desire was for a room temperature process. Using IGZO source/drain contacts further improved the transparency, but their electrical characteristics are still under investigation. The insets in Fig. 1 shows two chips with working transistors; inset (C) showing metallized source and drain contacts and inset (D) with a transparent ITO contact.

Figure 2 illustrates typical dc drain current–drain voltage ( $I_{DS}$ - $V_{DS}$ ) curves for an IGZO TFT with the channel deposited at an oxygen partial pressure of 25 mTorr and 50 nm in thickness. It can be seen that the drain current exhibits pinch-off and current saturation, indicating that the TFT follows standard field effect transistor characteristics. The IGZO TFT is shown to be a  $n$ -type enhancement mode device and hard saturation is achieved, which means that the entire thickness of the IGZO channel layer is depleted of carriers.

A typical dc transfer characteristic [ $\log(I_{DS})$ - $V_{GS}$ ] and gate leakage current [ $\log(|I_G|)$ - $V_{GS}$ ] of a TFT with IGZO channel thickness of 50 nm and grown at a oxygen partial pressure of 25 mTorr are shown in Fig. 3. The curves indicate a low off state current of  $1 \times 10^{-11}$  A, and a drain current on/off ratio of  $5 \times 10^7$  was obtained. The subthreshold gate voltage swing  $S$  is given by the maximum slope in the transfer curve and was determined to be 200 mV/decade.

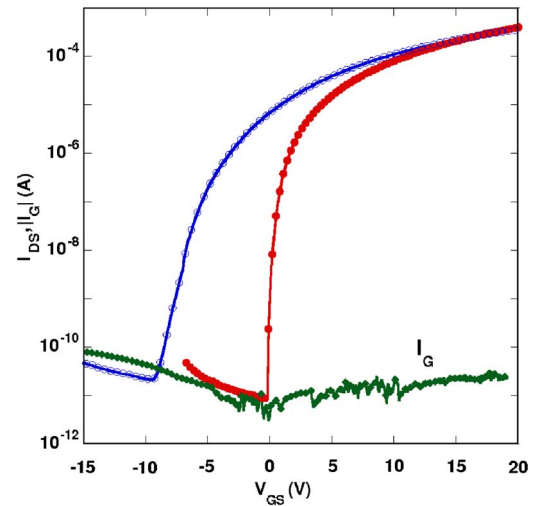


FIG. 3. (Color online)  $\log(I_{DS})$ - $V_{GS}$  and  $\log(I_G)$ - $V_{GS}$  at  $V_{DS}=20$  V for IGZO TFTs with ATO gate dielectric. IGZO channel deposited at oxygen partial pressure of 25 mTorr. TFT dimensions:  $L=100\ \mu\text{m}$  and  $W=400\ \mu\text{m}$ . Between the two  $I_{DS}$  curves, the IGZO channel thickness is varied, 50 nm (solid) and 75 nm (open).

The average capacitance of the ATO dielectric was measured to be  $55\ \text{nF cm}^{-2}$ . We extracted a threshold voltage of 2 V and a  $\mu_{\text{sat}}$  of  $11\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$ . This is comparable to the mobility reported for other oxide based TFTs.<sup>6,11,12</sup>

The IGZO channel layer was varied to assess its effect on the TFT behavior. Figure 3 also shows the transfer characteristics [ $\log(I_{DS})$ - $V_{GS}$ ] of a device with IGZO channel thickness of 75 nm, grown at 25 mTorr oxygen partial pressure. It is evident that the 75 nm channel device works as a depletion mode device and there is considerable drain current even when the gate bias is zero with a  $V_T$  of  $-2.5$  V. In the TFT with the thicker channel, the entire channel is not completely depleted of free carriers. The background current even at zero gate bias implies that a negative gate bias would be required to completely deplete the channel. This also shows that changing the channel thickness would be an effective way to engineer the threshold voltage,  $V_T$  of the TFTs.<sup>14,15</sup>

In general, TFT electrical behavior and hence the field effect mobility strongly depend on the gate dielectric material and thereby the dielectric/active layer interface. To evaluate this 200 nm,  $\text{SiN}_x$  was deposited on commercial ITO substrates (sheet resistance of  $100\ \Omega/\square$ ). For the channel layer IGZO films, 50 nm thick were grown at an oxygen partial pressure of 25 mTorr. The  $\log(I_{DS})$ - $V_{GS}$  characteristics for  $\text{SiN}_x$  and the ATO gate dielectric transistors are compared in Fig. 4(a). We observe that for the  $\text{SiN}_x$  TFT, the threshold voltage was lower compared to the ATO TFT. The effective field effect mobility for the  $\text{SiN}_x$  transistors, with a capacitance per unit area of  $22\ \text{nF cm}^{-2}$ , was  $5\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$  and the inverse subthreshold voltage slope was  $500\ \text{mV decade}^{-1}$  and inferior to the ATO transistors. We also observed a hysteresis in the forward and reverse voltage sweeps for the  $V_{GS}$ - $I_{DS}$  measurement for  $\text{SiN}_x$  gated transistors, while no significant hysteresis was observed in the ATO gated TFTs. Similar gate dielectric dependent observations have been reported in TFTs based on other material systems.<sup>3,11,16</sup>

Another reason for the importance of the gate dielectric is that these TFTs are essentially surface channel devices,

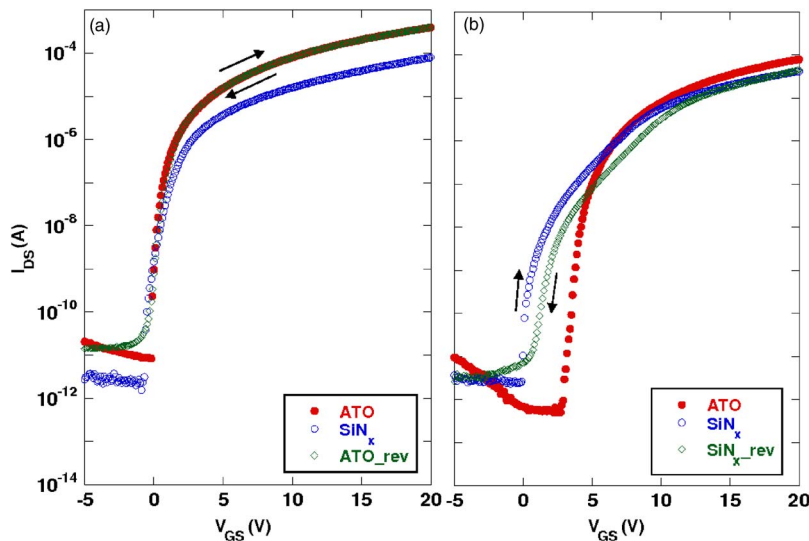


FIG. 4. Transfer characteristics [ $\log(I_{DS})-V_{GS}$ ] at  $V_{DS}=20$  V for IGZO TFTs with ATO and  $\text{SiN}_x$  gate dielectric both in the forward and reverse  $V_{GS}$  sweeps. Channel layer thickness of 50 nm and TFT dimensions of  $L=100$   $\mu\text{m}$  and  $W=400$   $\mu\text{m}$ . IGZO channel deposited at oxygen partial pressure of (a) 25 mTorr and (b) 40 mTorr. With ATO gate dielectric, the forward and reverse voltage sweeps were identical, as shown in (a). With  $\text{SiN}_x$  gate dielectrics a hysteresis was observed for the forward and reverse sweeps, as shown in (b). The oxygen partial pressure the film was grown at did not appear to influence the nature of the hysteresis.

whose action depends on the formation of an electron channel at the gate interface between the gate dielectric and active layer. It was observed that at higher gate bias, for example, greater than 24 V, that for a given step change in gate voltage the separation in saturation current  $I_{DS}$  curves decreased. This nonideality in the  $I_{DS}-V_{DS}$  characteristics implies a lower effective mobility at higher gate biases. This is consistent with carrier scattering at the interface as the electron channel narrows at a higher gate bias.<sup>9</sup>

Figure 4(b) also compares transistors with  $\text{SiN}_x$  and ATO gate dielectrics, except that the IGZO channel layer was deposited at a different oxygen partial pressure (40 mTorr). A few observations can be made from the  $\log(I_{DS})-V_{GS}$  curves. First, the threshold voltages are higher for both the  $\text{SiN}_x$  and ATO transistors grown at 40 mTorr compared to the TFTs grown at 25 mTorr. This higher  $V_T$  could be due to an increase in the defect or trap density at the gate dielectric/IGZO channel interface, but since the subthreshold gate swing remains almost unchanged this is not probable. However, since the 40 mTorr film inherently has lower carrier concentrations compared to the 25 mTorr film,<sup>17</sup> a larger portion of the gate voltage induced carriers would be required to compensate for the traps, presumably increasing the  $V_T$ . Secondly, the drain current for the 40 mTorr IGZO TFTs is considerably lower compared to the 25 mTorr IGZO TFTs, and the extracted effective field effect mobilities were 4 and 3.5  $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$  for the  $\text{SiN}_x$  and ATO transistors, respectively. We have reported a monotonically decreasing Hall mobility of the IGZO films with an increase in the deposition oxygen partial pressure and the field effect mobility scales well with these data.<sup>17</sup>

It should be pointed out that the entire processing of these TFTs is at room temperature. This is of major advantage for processing on flexible polymeric substrates. It has been shown in other systems based on amorphous active layers that a postprocessing annealing has an effect of increasing the effective mobilities of the TFTs.<sup>10</sup> This has been attributed to improved semiconductor-insulator interface or improvement in local atomic rearrangement. Either way this gives us a wider process window for the IGZO TFTs to achieve potentially higher effective mobilities depending on the application requirement.

To summarize, IGZO deposited by PLD at room temperature is used as a channel in transparent TFTs. The devices are transparent throughout the visible spectrum and exhibit good electrical characteristics. It was shown that the channel layer thickness could be used to vary the threshold voltage of the TFTs. The effect of the gate dielectric to optimize the electrical behavior was explored. The good electrical characteristics along with room temperature processing and high transparency make IGZO TFTs a viable candidate for flexible transparent electronics.

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