

Bias stress stability of indium gallium zinc oxide channel based transparent thin film transistors

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(Received 16 October 2007; accepted 26 November 2007; published online 23 January 2008)

The effects of bias stress on transistor performance are important when considering nontraditional channel materials for thin film transistors. Applying a gate bias stress to indium gallium zinc oxide transparent thin film transistors was found to induce a parallel threshold voltage shift without changing the field effect mobility or the subthreshold gate voltage swing. The threshold voltage change is logarithmically dependent on the duration of the bias stress implying a charge tunneling mechanism resulting in trapped negative charge screening the applied gate voltage. © 2008 American Institute of Physics. [DOI: 10.1063/1.2824758]

Over the past few years, great progress has been made in the field of thin film transistors (TFTs) using a wide variety of different channel materials. When examining the requirements for large area deposition and mechanical stability when placed on flexible substrates, amorphous oxide semiconductors (AOSs) appear especially promising.^{1,2} Compared to traditional amorphous semiconductors such as *a*-Si and organic thin film transistor materials, AOS based TFTs have clearly superior electron mobilities.³ Transistors with good characteristics with 1–2 V threshold voltages, current on/off ratios of 10^7 – 10^8 , electron mobilities being 10 – 50 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$, and subthreshold slopes of 0.1 – 0.2 V decade⁻¹ have been reported.^{3–5} However, for applications, it is necessary to understand how these devices behave under bias stress.

It is well established for *a*-Si and other thin film transistor materials/devices that prolonged application of gate bias on the TFTs can result in the deterioration of the current-voltage characteristics. This effect could be manifested as a change in the field effect mobility, a change in the subthreshold slope, or as a shift in threshold voltage.^{6–8} This is commonly referred to as the bias stress effect and has been observed in *a*-Si:H,⁹ poly-Si,¹⁰ and several organic TFTs.^{11–13} In the literature, several mechanisms have been proposed to explain the bias stress effect.^{9,13}

Though AOS based TFTs have been extensively studied by various groups, very few experimental work has been reported on the bias stress effect on AOS TFTs.^{14,15} In this paper, we focus on indium gallium zinc oxide (IGZO) channel TFTs that are amorphous, and deposited at room temperature and fabricated without any annealing or material passivation steps, and report the results of bias stress measurements. This study reveals that the effects of a constant gate bias stress and the resulting shifts in threshold voltage can be explained using a simple charge trapping model. This indicates that IGZO is robust as a channel material and that with the appropriate choice of the gate dielectric, where the interface trap density can be controlled, TFTs that are transparent in the visible spectrum should find numerous applications.

Transparent IGZO ($\text{In}_2\text{O}_3:\text{Ga}_2\text{O}_3:\text{ZnO}$ = 1:1:10 mol %) TFTs were fabricated using a bottom gated

configuration with indium tin oxide (ITO), atomic layer deposited AlO_x and TiO_x (ATO), IGZO and ITO as the gate electrode, dielectric, channel and source and drain electrodes, respectively. The fabrication details have been discussed elsewhere.⁵ The IGZO channel and the ITO source and drain were deposited using pulsed laser deposition (PLD) at room temperature. Good transistor characteristics were obtained without any annealing of the films. The oxygen pressure used during the IGZO deposition was set at 25 mTorr. Transistors used in the study operate as a *n*-channel enhancement mode device and exhibit good characteristics.⁵ The TFT dimension used for this study was 100×400 μm^2 ($L \times W$). All the bias stress measurements were carried out at room temperature, in air and in the dark, and a “virgin” device was used for each stressing condition. Gate bias stress was carried out for a predetermined time with the bias stress voltage in the linear regime using a V_{DS} of 1 V instead of the saturation regime where the effect of bias stress on the threshold voltage shift is smaller.⁸ The transfer characteristics were measured before and after applying the stress in a dual sweep mode. The threshold voltage V_{th} was extracted from the $\sqrt{I_{\text{DS}}}$ vs V_{GS} plots. The *I*-*V* characteristics of the transistors were measured on a semiconductor parameter analyzer, Keithley 4200, and the *C*-*V* measurements were carried out on an LCR meter, HP 4284A.

Figure 1(a) shows two transfer characteristics of the same TFT device. After the first gate voltage sweep, the gate electrode was stressed at 30 V for 500 s. Following this, the second gate voltage sweep was performed. It can be seen that the transfer characteristics [$\log(I_{\text{DS}}) - V_{\text{GS}}$] of the device before and after the bias stress have a similar shape except for a parallel shift along the gate voltage axis in the positive direction; this is the typical threshold voltage shift seen in TFTs after bias stressing. Figure 1(a) also shows that the subthreshold slope of the device (~ 0.25 V decade⁻¹) does not change even after the device has undergone bias stressing. This indicates that no additional defect states are created at the channel/dielectric interface after the device was stressed.¹³

Figure 1(b) shows the plot of the square root of the drain current as a function of the applied gate bias. From the plot, it is clear that the slope of the linear part of the curve, which is proportional to the field effect mobility in the saturation regime, is similar for both curves. The extracted mobility (~ 14 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$) seems to remain unaltered even after the

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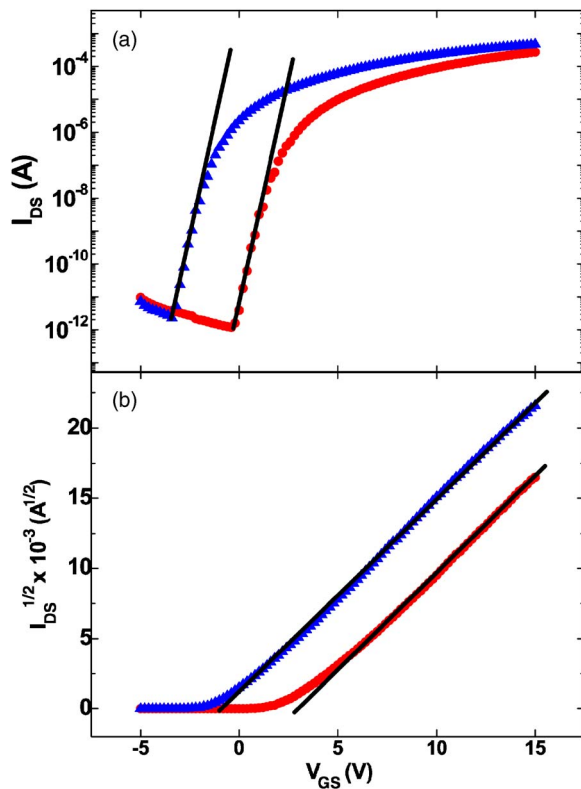


FIG. 1. (Color online) Effect of bias stress on the drain current, the field effect mobility, and the subthreshold voltage swing of the TFT. 30 V bias stress was applied on the gate electrode for 500 s, while V_{DS} was kept at 1 V. The I_{DS} - V_{GS} sweep was done at $V_{DS}=15$ V. (\blacktriangle —prestress and \bullet —poststress.) Only the forward sweep has been plotted.

application of gate bias stress. The phenomenon of a positive threshold voltage shift with an applied positive gate bias results from negative charge being trapped at the channel/dielectric interface or getting injected into the gate dielectric. The positive threshold voltage shift is then explained by the negative charge screening the applied gate voltage. The lower effective gate bias results in a smaller current flowing through the channel, thus a larger positive voltage is required for the device to turn on and reach saturation.

Figure 2 shows the room temperature dc C - V measurement of the ITO/ATO/IGZO/ITO capacitor structure. The capacitor was subjected to three back-to-back hysteresis loop sweeps $V_G=-10$ to 10, -20 to 20, and -30 to 30 V. From Fig. 2, we observe that the flat band voltage V_{FB} shifts successively to more positive voltage for each hysteresis loop during the return sweep. This is additional evidence that negative carriers are trapped at the channel/dielectric interface or injected into the dielectric from the IGZO channel. Also note that the forward sweeps of curves, -20 to 20 and -30 to 30 V, fall on the previous curve reverse sweeps (i.e., -10 to 10 V and -20 to 20 V, respectively). This indicates that when a negative bias is applied to the gate, no positive charges are injected from the IGZO channel into the gate dielectric and the capacitor maintains its characteristics from the positive part of the previous hysteresis loop. The slope of the curves in the transition region from accumulation to depletion is the same as that from depletion to accumulation, indicating that the bias stress does not change the trap density at the channel/dielectric interface.

This was further verified by applying negative voltages as a bias stress. Figure 3 compares two TFTs: one having

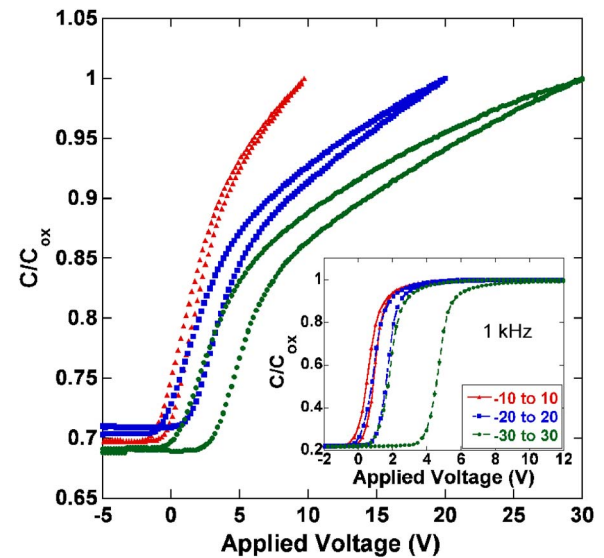


FIG. 2. (Color online) Hysteresis behavior of ITO/ATO/IGZO/ITO capacitor structure. Hysteresis sweeps -10 to 10, -20 to 20, and -30 to 30 V were made consecutively. The size of the capacitor pad is $200 \times 1600 \mu\text{m}^2$. The directions of the forward and reverse sweeps are indicated. Measurements were carried out at 1 MHz. The inset shows the 1 kHz data; note the expanded scale in the inset.

been subjected to a positive gate bias stress, while the other undergoes a negative gate bias stress. It can be seen that, as expected, the positive bias stress causes a positive threshold voltage shift ΔV_{th} , where $\Delta V_{th}=V_{th}(t)-V_{th}(t=0)$, while the negative gate bias stress does not change the threshold voltage, and the transfer curve of the stressed TFT overlaps that of the unstressed TFT. This is an indication that when a negative bias is applied to the gate, the transistor channel is depleted of electrons at the channel/dielectric interface and no mobile charges are available for the charge trapping and tunneling process.

The dependence of the threshold voltage shift on the duration of the applied gate bias is plotted in Fig. 4 for different gate stress voltages. From the plot, a linear relationship between ΔV_{th} and logarithmic time can be seen. The

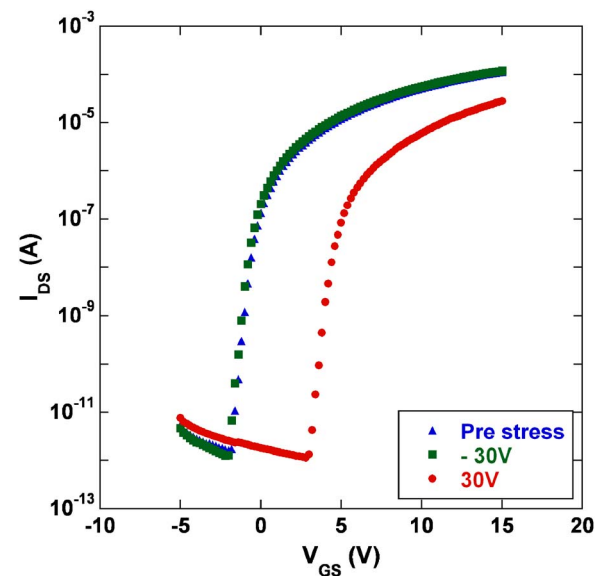


FIG. 3. (Color online) Comparison of the effect of a positive and a negative gate bias stress on the transfer characteristics. Stress duration was 500 s, $V_{DS}=1$ V. The I_{DS} - V_{GS} sweep was done at $V_{DS}=20$ V.

inset shows that this model is predictive of the voltage threshold shift for long stress durations of up to 24 h. This dependence is indicative of charge trapping phenomenon.¹⁵ The relationship can be modeled by quantifying the total charge that get trapped at the channel/dielectric interface or in the dielectric for any given time t . Given the material parameters (work function, capacitance, etc.) are invariant during biasing, the ΔV_{th} can be expressed as

$$\Delta V_{th}(t) = Q(t)/C_{ox}, \quad (1)$$

where $Q(t)$ is the total charge trapped and C_{ox} is the capacitance per unit area of the gate dielectric. By assuming a uniform distribution of traps in the dielectric, an expression for the total trapped charge is obtained by integrating over time and thickness of the gate dielectric in which traps are present,¹⁶

$$Q(t) = \int_0^t dt' \int_0^x dx' N_{tr} \varpi(x') \exp[-\varpi(x')t'], \quad (2)$$

where N_{tr} is the density of traps in the dielectric and $\varpi(x) = \varpi_0 \exp(-x/\lambda)$ is the time independent tunneling probability, where the tunneling constant λ is the product of the applied gate voltage and dielectric material parameters. The solution of the above equation leads to the ΔV_{th} expression given below,

$$\Delta V_{th} = r_0 \log\left(\frac{t}{t_0}\right), \quad (3)$$

where r_0 is a decay rate constant which is proportional to the product of N_{tr} (cm^{-3}) and λ (cm). Since λ is dependent on the applied gate voltage, higher bias stresses will result in more charge trapping, larger decay rate constants, and larger voltage shifts.

One way to reduce the threshold voltage shift during bias stressing would be to reduce the mobile carriers in the channel. Films grown at a higher oxygen partial pressure tend to have lower carrier concentration.¹⁷ The effect of IGZO growth conditions on ΔV_{th} is also shown in Fig. 4. We can clearly see that the TFT fabricated with a 40 mTorr channel is less sensitive to gate bias stress with lower threshold voltage shifts. Varying the oxygen partial pressure during deposition of the channel slightly changes the composition of the film.¹⁷ This requires more investigation, but it could affect the channel/dielectric interface by changing the density of the interface states resulting in a reduction in the threshold voltage shifts. In general, the decay rate constant appears to be a strong function of the applied gate bias.

Annealing the IGZO films at temperatures as low as 200 °C in atmosphere for a few minutes leads to a drop in the carrier concentration.¹⁷ The highest temperature the as fabricated transistors were exposed to during processing is a 95 °C photoresist bake step. To investigate the effect of post-deposition annealing, TFTs fabricated with a 25 mTorr channel were annealed at 200 °C for 10 min in atmosphere. Bias stress data were measured before and after the annealing and plotted in Fig. 4. It was found that the ΔV_{th} reduced from 4.6 to 3 V for a bias stress of 30 V and duration of 1000 s. This suggests that improvements in the channel/dielectric interface can be obtained, via reduction in charge trapping defects, with some improvement also resulting from a reduction in carrier concentration.

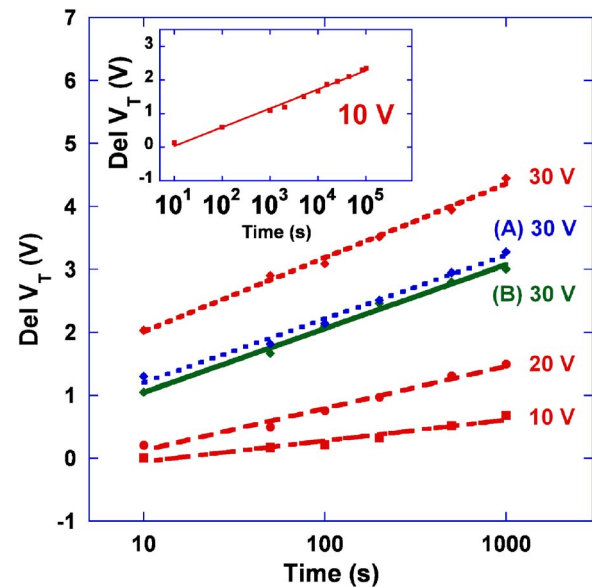


FIG. 4. (Color online) Logarithmic dependence of the threshold voltage shift ΔV_{th} with the bias stress duration. The effect of the gate voltage is seen as well (■—10 V, ●—20 V, and ◆—30 V). ΔV_{th} for TFTs bias stressed at 30 V based on an IGZO channel grown at [(A)◆] 40 mTorr and [(B)◆] 25 mTorr and annealed in air for 10 min at 200 °C are plotted as well. The inset shows the effect of a 10 V gate bias for stresses applied up to 24 h.

In conclusion, we have investigated the effects of bias stress on IGZO thin film transistors. A threshold voltage shift (ΔV_{th}) was observed as a result of bias stress, and this shift was quantified as a function of bias stress voltage and duration. Both I - V and C - V measurements were used to determine that the voltage instability arises due to the process of charge trapping in the channel/dielectric interface or in the dielectric due to bias stressing.

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